Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claim 74, as follows:

Listing of Claims:

1-66. (Cancelled)

67. (Previously presented) In a memory device, a method of adjusting the timing of at least two digital signals of a plurality of digital signals applied to a signal bus relative to a common clock signal, each digital signal responsive to a respective internal clock signal, the method comprising:

for at least two of the plurality of digital signals, determining a level of timing compensation for each of the respective internal clock signals to compensate for the respective signal skew determined for each of the two digital signals;

storing for each of the two digital signals a respective value indicative of the level of compensation for each of the respective internal clock signals; and

adjusting the timing of each of the respective internal clock signals relative to the common clock signal according to the respective value stored for each of the two digital signals.

68. (Previously presented) The method of claim 67 wherein determining the level of timing compensation, storing a respective value, and adjusting the timing is performed for each of the plurality of digital signals.

69. (Previously presented) The method of claim 67 wherein storing for each of the two digital signals a respective value comprises storing a first value for a first of the two digital signals and storing a second value different than the first value for a second of the two digital signals.

70. (Previously presented) The method of claim 67 wherein the plurality of digital signals comprise data signals.

71. (Previously presented) The method of claim 67 wherein determining the level of timing compensation for each of the respective internal clock signals comprises:

repetitively applying digital signals having expected values for each of the two digital signals;

evaluating the digital signal captured responsive to a data clock signal based on the common clock signal to determine if the captured digital signal has the expected value;

identifying levels of timing compensation that cause the associated digital signal having the expected value to be captured; and

selecting for storage one of the levels of timing compensation for each digital signal that caused the associated digital signal having the expected value to be captured.

72. (Previously presented) The method of claim 71 wherein identifying the levels of timing compensation that cause the associated digital signal having the expected value to be captured comprises:

reading an initial value from a storage circuit;

incrementing or decrementing the initial value to adjust the level of timing compensation;

storing the incremented or decremented value in the storage circuit;

applying the digital signals having expected values based on the timing according to the incremented or decremented value; and

evaluating whether the digital signal captured responsive to the data clock signal has the expected value.

73. (Previously presented) The method of claim 71 wherein evaluating the captured digital signal to determine if the digital signal has the expected value comprises:

capturing the digital signal responsive to the data clock signal;

generating expected values for the digital signal responsive to the values of the captured digital signal; and

determining that the digital signal was successfully captured when the values of the captured digital signal corresponds to the generated expected values for the digital signal.

74. (Currently amended) A method for compensating for timing skew of at least some a plurality of digital signals relative to a common clock signal, each one of the digital signals responsive to a respective timing clock signal, the method comprising:

generating a plurality of phase adjusted clock signals, each of the plurality of phase adjusted clock signals having a different phase relationship relative to the common clock signal;

for <u>each of</u> at least two of the plurality of the digital signals, selecting one of the plurality of phase adjusted clock signals to act as the respective timing clock signal in order to compensate for the respective timing skew of the digital signal;

storing for each of the two digital signals a respective compensation value indicative of the respective selected phase adjusted clock signal; and

according to the respective compensation value stored for each of the two digital signals, applying the selected phase adjusted clock signal as the respective timing clock signal.

75. (Previously presented) The method of claim 74 wherein selecting one of the plurality of phase adjusted clock signals, storing a respective compensation value, and applying the selected phase adjusted clock signal is performed for each of the plurality of digital signals.

76. (Previously presented) The method of claim 74 wherein storing for each of the two digital signals a respective compensation value comprises storing a first compensation value for a first of the two digital signals and storing a second compensation value different than the first value for a second of the two digital signals.

77. (Previously presented) The method of claim 74 wherein the plurality of digital signals comprise data signals.

78. (Previously presented) The method of claim 74, further comprising:

repetitively applying digital signals having expected values for each of the two digital signals;

evaluating the digital signal captured responsive to a data clock signal based on the common clock signal to determine if the captured digital signal has the expected value;

identifying levels of timing compensation that cause the associated digital signal having the expected value to be captured; and

selecting for storage one of the levels of timing compensation for each digital signal that caused the associated digital signal having the expected value to be captured.

79. (Previously presented) The method of claim 78 wherein identifying the levels of timing compensation that cause the associated digital signal having the expected value to be captured comprises:

reading an initial value from a storage circuit;

incrementing or decrementing the initial value to adjust the level of timing compensation;

storing the incremented or decremented value in the storage circuit;

applying the digital signals having expected values based on the timing according to the incremented or decremented value; and

evaluating whether the digital signal captured responsive to the data clock signal has the expected value.

80. (Previously presented) The method of claim 78 wherein evaluating the captured digital signal to determine if the digital signal has the expected value comprises:

capturing the digital signal responsive to the data clock signal;

generating expected values for the digital signal responsive to the values of the captured digital signal; and

determining that the digital signal was successfully captured when the values of the captured digital signal corresponds to the generated expected values for the digital signal.

81. (Previously presented) A timing skew compensation circuit for generating a plurality of skew compensated latch clock signals that are applied to a corresponding plurality of latch circuits to compensate for timing skew of a corresponding plurality of digital signals relative to a common clock signal, the timing skew compensation circuit comprising:

a clock generator having an input node at which the common clock signal is applied and further having a plurality of output nodes at which a plurality of phase adjusted clock signals are provided, each phase adjusted clock signal having a different phase relationship relative to a common clock signal applied to the clock generator;

a plurality of selection circuits, each selection circuit having a plurality of input nodes coupled to the plurality of output nodes of the clock generator to receive the plurality of phase adjusted clock signals, each selection circuit further having a control node at which control signals are applied and having an output node at which one of the plurality of phase adjusted clock signals is provided as a skew compensated latch clock signal based on the control signals applied to the control node;

a plurality of registers, each register coupled to the control node of a corresponding one of the plurality of the selection circuits to provide a respective stored value as the control signals to the respective selection circuit; and

a control circuit coupled to each of the plurality of registers, the control circuit generating for each of the registers a compensation value for storage that when provided to the respective selection circuit as the control signal compensates for the timing skew associated with the respective digital signal.

82. (Previously presented) The timing skew compensation circuit of claim 81 wherein the common clock signal comprises a read clock signal and the plurality of digital signals comprises a plurality of data signals.

83. (Previously presented) The timing skew compensation circuit of claim 81 wherein the control circuit comprises:

a command buffer and address capture circuit adapted to latch and output command-address signals applied on a command address bus;

a command decoder and sequencer coupled to the output of the command buffer and address capture circuit that generates a plurality of control signals responsive to the latched command-address signals, and generates a signal timing adjustment command responsive to adjustment signals included in the latched command-address signals, the signal timing adjustment command including information identifying a particular digital signal of the plurality of digital signals; and

an up/down counter-controller coupled to the command decoder and sequencer to receive the signal timing adjustment command, and coupled to the registers, the counter-controller adjusting the value stored in the register associated with the identified digital signal responsive to the signal timing adjustment command.

84. (Previously presented) The timing skew compensation circuit of claim 83 wherein the counter-controller adjusts the value stored in each register by first reading a presently stored value, incrementing or decrementing the presently stored value responsive to the signal timing adjustment command to develop a new value, and thereafter storing the new value in the register.

85. (Previously presented) The timing skew compensation circuit of claim 83 wherein the control circuit further comprises a read pattern generator that generates synchronization digital signals to be applied to inputs of the latch circuits, each signal being a repeating pseudo-random bit sequence.

86. (Previously presented) The timing skew compensation circuit of claim 81 wherein the clock generator comprises a delay-locked loop circuit.

87. (Previously presented) A clock signal generator for generating a plurality of skew compensated latch clock signals that are applied to a corresponding plurality of latch circuits to compensate for the timing skews of a corresponding plurality of digital signals relative to a common clock signal, the clock signal generator comprising:

a plurality of multiplexer circuits, each multiplexer circuit having a plurality of input nodes to which a plurality of phase adjusted clock signals are applied, each phase adjusted clock signal having a different phase relationship relative to the common clock signal, each multiplexer circuit further having a control node at which control signals are applied and having an output node at which one of the plurality of phase adjusted clock signals is provided as a skew compensated latch clock signal to a respective one of the latch circuits based on the control signals applied to the control node;

a plurality of registers, each register coupled to the control node of a respective one of the plurality of multiplexer circuits to provide a timing compensation value as the control signals to the respective multiplexer circuit; and

a control circuit coupled to each of the plurality of registers, the control circuit generating a timing compensation value for each register that compensates for the timing skew of the respective digital signal.

88. (Previously presented) The clock signal generator of claim 87 wherein the common clock signal comprises a read clock signal and the plurality of digital signals comprises a plurality of data signals.

89. (Previously presented) The clock signal generator of claim 87 wherein the control circuit comprises:

a command buffer and address capture circuit adapted to latch and output command-address signals applied on a command address bus;

a command decoder and sequencer coupled to the output of the command buffer and address capture circuit that generates a plurality of control signals responsive to the latched command-address signals, and generates a signal timing adjustment command responsive to adjustment signals included in the latched command-address signals, the signal timing adjustment command including information identifying a particular digital signal of the plurality of digital signals; and

an up/down counter-controller coupled to the command decoder and sequencer to receive the signal timing adjustment command, and coupled to the registers, the counter-controller adjusting the timing compensation value stored in the register associated with the identified digital signal responsive to the signal timing adjustment command.

90. (Previously presented) The clock signal generator of claim 89 wherein the counter-controller adjusts the timing compensation value stored in each register by first reading a presently stored timing compensation value, incrementing or decrementing the presently stored timing compensation value responsive to the signal timing adjustment command to develop a new timing compensation value, and thereafter storing the new timing compensation value in the register.

91. (Previously presented) The clock signal generator of claim 89 wherein the control circuit further comprises a read pattern generator that generates synchronization digital signals to be applied to inputs of the latch circuits, each signal being a repeating pseudo-random bit sequence.

92. (Previously presented) The clock signal generator of claim 87, further comprising a clock generator having an input node at which the common clock signal is applied and further having a plurality of output nodes coupled to the input nodes of the plurality of multiplexer circuits to provide the plurality of phase adjusted clock signals, each phase adjusted clock signal having a known phase relationship relative to the common clock signal.

93. (Previously presented) A memory device, comprising:

at least one array of memory cells adapted to store data at a location determined by a row address and a column address;

a control circuit adapted to receive external control signals and operable in response to the external control signals to generate a plurality of internal control signals;

a row address circuit adapted to receive and decode the row address, and select a row of memory cells corresponding to the row address responsive to the internal control signals;

a column address circuit adapted to receive or apply data to at least one of the memory cells in the selected row corresponding to the column address responsive to the internal control signals;

a write data path circuit adapted to couple data between a data bus and the column address circuit responsive to the internal control signals; and

a read data path circuit adapted to couple data between the data bus and the column address circuit responsive to the internal control signals, the read data path circuit comprising a timing skew compensation circuit for generating a plurality of skew compensated latch clock signals that are applied to a corresponding plurality of latch circuits to compensate for timing skew of a corresponding plurality of digital signals relative to a common clock signal, the timing skew compensation circuit comprising:

a clock generator having an input node at which the common clock signal is applied and further having a plurality of output nodes at which a plurality of phase adjusted clock signals are provided, each phase adjusted clock signal having a different phase relationship relative to a common clock signal applied to the clock generator;

a plurality of selection circuits, each selection circuit having a plurality of input nodes coupled to the plurality of output nodes of the clock generator to receive the plurality of phase adjusted clock signals, each selection circuit further having a control node at which control signals are applied and having an output node at which one of the plurality of phase adjusted clock signals is provided as a skew compensated latch clock signal based on the control signals applied to the control node;

a plurality of registers, each register coupled to the control node of a corresponding one of the plurality of the selection circuits to provide a respective stored value as the control signals to the respective selection circuit; and

a control circuit coupled to each of the plurality of registers, the control circuit generating for each of the registers a compensation value for storage that when provided to the respective selection circuit as the control signal compensates for the timing skew associated with the respective digital signal.

94. (Previously presented) The memory device of claim 93 wherein the common clock signal comprises a read clock signal and the plurality of digital signals comprises a plurality of data signals.

95. (Previously presented) The memory device of claim 93 wherein the control circuit of the timing skew compensation circuit comprises:

a command buffer and address capture circuit adapted to latch and output command-address signals applied on a command address bus;

a command decoder and sequencer coupled to the output of the command buffer and address capture circuit that generates a plurality of control signals responsive to the latched command-address signals, and generates a signal timing adjustment command responsive to adjustment signals included in the latched command-address signals, the signal timing adjustment command including information identifying a particular digital signal of the plurality of digital signals; and

an up/down counter-controller coupled to the command decoder and sequencer to receive the signal timing adjustment command, and coupled to the registers, the counter-controller adjusting the value stored in the register associated with the identified digital signal responsive to the signal timing adjustment command.

96. (Previously presented) The memory device of claim 95 wherein the counter-controller adjusts the value stored in each register by first reading a presently stored

value, incrementing or decrementing the presently stored value responsive to the signal timing adjustment command to develop a new value, and thereafter storing the new value in the register.

97. (Previously presented) The memory device of claim 95 wherein the control circuit further comprises a read pattern generator that generates synchronization digital signals to be applied to inputs of the latch circuits, each signal being a repeating pseudo-random bit sequence.

98. (Previously presented) The memory device of claim 93 wherein the clock generator of the timing skew compensation circuit comprises a delay-locked loop circuit.

99. (Previously presented) A memory device, comprising:

at least one array of memory cells adapted to store data at a location determined by a row address and a column address;

a control circuit adapted to receive external control signals and operable in response to the external control signals to generate a plurality of internal control signals;

a row address circuit adapted to receive and decode the row address, and select a row of memory cells corresponding to the row address responsive to the internal control signals;

a column address circuit adapted to receive or apply data to at least one of the memory cells in the selected row corresponding to the column address responsive to the internal control signals;

a write data path circuit adapted to couple data between a data bus and the column address circuit responsive to the internal control signals; and

a read data path circuit adapted to couple data between the data bus and the column address circuit responsive to the internal control signals, the read data path circuit comprising a clock signal generator for generating a plurality of skew compensated latch clock signals that are applied to a corresponding plurality of latch circuits to compensate for the timing skews of a corresponding plurality of digital signals relative to a common clock signal, the clock signal generator comprising:

a plurality of multiplexer circuits, each multiplexer circuit having a plurality of input nodes to which a plurality of phase adjusted clock signals are applied, each phase adjusted clock signal having a different phase relationship relative to the common clock signal, each multiplexer circuit further having a control node at which control signals are applied and having an output node at which one of the plurality of phase adjusted clock signals is provided as a skew compensated latch clock signal to a respective one of the latch circuits based on the control signals applied to the control node;

a plurality of registers, each register coupled to the control node of a respective one of the plurality of multiplexer circuits to provide a timing compensation value as the control signals to the respective multiplexer circuit; and

a control circuit coupled to each of the plurality of registers, the control circuit generating a timing compensation value for each register that compensates for the timing skew of the respective digital signal.

100. (Previously presented) The memory device of claim 99 wherein the common clock signal comprises a read clock signal and the plurality of digital signals comprises a plurality of data signals.

101. (Previously presented) The memory device of claim 99 wherein the control circuit of the clock signal generator comprises:

a command buffer and address capture circuit adapted to latch and output command-address signals applied on a command address bus;

a command decoder and sequencer coupled to the output of the command buffer and address capture circuit that generates a plurality of control signals responsive to the latched command-address signals, and generates a signal timing adjustment command responsive to adjustment signals included in the latched command-address signals, the signal timing adjustment command including information identifying a particular digital signal of the plurality of digital signals; and

an up/down counter-controller coupled to the command decoder and sequencer to receive the signal timing adjustment command, and coupled to the registers, the counter-controller adjusting the timing compensation value stored in the register associated with the identified digital signal responsive to the signal timing adjustment command.

102. (Previously presented) The memory device of claim 101 wherein the counter-controller adjusts the timing compensation value stored in each register by first reading a presently stored timing compensation value, incrementing or decrementing the presently stored timing compensation value responsive to the signal timing adjustment command to develop a new timing compensation value, and thereafter storing the new timing compensation value in the register.

103. (Previously presented) The memory device of claim 101 wherein the control circuit further comprises a read pattern generator that generates synchronization digital signals to be applied to inputs of the latch circuits, each signal being a repeating pseudo-random bit sequence.

104. (Previously presented) The memory device of claim 99 wherein the clock signal generator further comprises a clock generator having an input node at which the common clock signal is applied and further having a plurality of output nodes coupled to the input nodes of the plurality of multiplexer circuits to provide the plurality of phase adjusted clock signals, each phase adjusted clock signal having a known phase relationship relative to the common clock signal.

105. (Previously presented) A processing system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system; and

a memory device coupled to the processor, comprising,

at least one array of memory cells adapted to store data at a location determined by a row address and a column address;

a control circuit adapted to receive external control signals and operable in response to the external control signals to generate a plurality of internal control signals;

a row address circuit adapted to receive and decode the row address, and select a row of memory cells corresponding to the row address responsive to the internal control signals;

a column address circuit adapted to receive or apply data to at least one of the memory cells in the selected row corresponding to the column address responsive to the internal control signals;

a write data path circuit adapted to couple data between a data bus and the column address circuit responsive to the internal control signals; and

a read data path circuit adapted to couple data between the data bus and the column address circuit responsive to the internal control signals, the read data path circuit comprising a timing skew compensation circuit for generating a plurality of skew compensated latch clock signals that are applied to a corresponding plurality of latch circuits to compensate for timing skew of a corresponding plurality of digital signals relative to a common clock signal, the timing skew compensation circuit comprising:

a clock generator having an input node at which the common clock signal is applied and further having a plurality of output nodes at which a plurality of phase adjusted clock signals are provided, each phase adjusted clock signal having a different phase relationship relative to a common clock signal applied to the clock generator;

a plurality of selection circuits, each selection circuit having a plurality of input nodes coupled to the plurality of output nodes of the clock generator to receive the plurality of phase adjusted clock signals, each selection circuit further having a control node at which control signals are applied and having an output node at which one of the plurality of

phase adjusted clock signals is provided as a skew compensated latch clock signal based on the control signals applied to the control node;

a plurality of registers, each register coupled to the control node of a corresponding one of the plurality of the selection circuits to provide a respective stored value as the control signals to the respective selection circuit; and

a control circuit coupled to each of the plurality of registers, the control circuit generating for each of the registers a compensation value for storage that when provided to the respective selection circuit as the control signal compensates for the timing skew associated with the respective digital signal.

106. (Previously presented) The processing system of claim 105 wherein the common clock signal comprises a read clock signal and the plurality of digital signals comprises a plurality of data signals.

107. (Previously presented) The processing system of claim 105 wherein the control circuit of the timing skew compensation circuit comprises:

a command buffer and address capture circuit adapted to latch and output command-address signals applied on a command address bus;

a command decoder and sequencer coupled to the output of the command buffer and address capture circuit that generates a plurality of control signals responsive to the latched command-address signals, and generates a signal timing adjustment command responsive to adjustment signals included in the latched command-address signals, the signal timing adjustment command including information identifying a particular digital signal of the plurality of digital signals; and

an up/down counter-controller coupled to the command decoder and sequencer to receive the signal timing adjustment command, and coupled to the registers, the counter-controller adjusting the value stored in the register associated with the identified digital signal responsive to the signal timing adjustment command.

108. (Previously presented) The processing system of claim 107 wherein the counter-controller adjusts the value stored in each register by first reading a presently stored value, incrementing or decrementing the presently stored value responsive to the signal timing adjustment command to develop a new value, and thereafter storing the new value in the register.

109. (Previously presented) The processing system of claim 107 wherein the control circuit further comprises a read pattern generator that generates synchronization digital signals to be applied to inputs of the latch circuits, each signal being a repeating pseudo-random bit sequence.

110. (Previously presented) The processing system of claim 105 wherein the clock generator of the timing skew compensation circuit comprises a delay-locked loop circuit.

111. (Previously presented) A processing system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system; and

a memory device coupled to the processor, comprising,

at least one array of memory cells adapted to store data at a location determined by a row address and a column address;

a control circuit adapted to receive external control signals and operable in response to the external control signals to generate a plurality of internal control signals;

a row address circuit adapted to receive and decode the row address, and select a row of memory cells corresponding to the row address responsive to the internal control signals;

a column address circuit adapted to receive or apply data to at least one of the memory cells in the selected row corresponding to the column address responsive to the internal control signals;

a write data path circuit adapted to couple data between a data bus and the column address circuit responsive to the internal control signals; and

a read data path circuit adapted to couple data between the data bus and the column address circuit responsive to the internal control signals, the read data path circuit comprising a clock signal generator for generating a plurality of skew compensated latch clock signals that are applied to a corresponding plurality of latch circuits to compensate for the timing skews of a corresponding plurality of digital signals relative to a common clock signal, the clock signal generator comprising:

a plurality of multiplexer circuits, each multiplexer circuit having a plurality of input nodes to which a plurality of phase adjusted clock signals are applied, each phase adjusted clock signal having a different phase relationship relative to the common clock signal, each multiplexer circuit further having a control node at which control signals are applied and having an output node at which one of the plurality of phase adjusted clock signals is provided as a skew compensated latch clock signal to a respective one of the latch circuits based on the control signals applied to the control node;

a plurality of registers, each register coupled to the control node of a respective one of the plurality of multiplexer circuits to provide a timing compensation value as the control signals to the respective multiplexer circuit; and

a control circuit coupled to each of the plurality of registers, the control circuit generating a timing compensation value for each register that compensates for the timing skew of the respective digital signal.

112. (Previously presented) The processing system of claim 111 wherein the common clock signal comprises a read clock signal and the plurality of digital signals comprises a plurality of data signals.

113. (Previously presented) The processing system of claim 111 wherein the control circuit of the clock signal generator comprises:

a command buffer and address capture circuit adapted to latch and output command-address signals applied on a command address bus;

a command decoder and sequencer coupled to the output of the command buffer and address capture circuit that generates a plurality of control signals responsive to the latched command-address signals, and generates a signal timing adjustment command responsive to adjustment signals included in the latched command-address signals, the signal timing adjustment command including information identifying a particular digital signal of the plurality of digital signals; and

an up/down counter-controller coupled to the command decoder and sequencer to receive the signal timing adjustment command, and coupled to the registers, the counter-controller adjusting the timing compensation value stored in the register associated with the identified digital signal responsive to the signal timing adjustment command.

114. (Previously presented) The processing system of claim 113 wherein the counter-controller adjusts the timing compensation value stored in each register by first reading a presently stored timing compensation value, incrementing or decrementing the presently stored timing compensation value responsive to the signal timing adjustment command to develop a new timing compensation value, and thereafter storing the new timing compensation value in the register.

115. (Previously presented) The processing system of claim 113 wherein the control circuit further comprises a read pattern generator that generates synchronization digital signals to be applied to inputs of the latch circuits, each signal being a repeating pseudo-random bit sequence.

116. (Previously presented) The processing system of claim 111 wherein the clock signal generator further comprises a clock generator having an input node at which the

common clock signal is applied and further having a plurality of output nodes coupled to the input nodes of the plurality of multiplexer circuits to provide the plurality of phase adjusted clock signals, each phase adjusted clock signal having a known phase relationship relative to the common clock signal.